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FORD GLOBAL TECHNOLOGIES, LLC.
FAIRLANE PLAZA SOUTH, SUITE 800
330 TOWN CENTER DRIVE
DEARBORN, MI 48126

EXAMINER	
PATEL, SHAMBHAVI K	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,801	BERTINI ET AL.	
	Examiner	Art Unit	
	Shambhavi Patel	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *06 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-24 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. **Claims 1, 3-6, 8-12, 14-19, and 21-24 are rejected under 35 U.S.C. 102(e)** as being anticipated by Heile et al, herein referred to as '**Heile' (US Patent No. 6,289,319)**.

As per **claim 1**, Heile is directed to a method for managing electrical schematic data comprising:

a. Creating a logical schematic for a part (column 6 lines 54-55, column 7 lines 14-22).

b. Creating a layout schematic for said part (column 7 lines 49-52). Heile teaches that before developing the design, a system specification for the design is obtained. The specification includes information on the pins, system functionality, timing restraints, etc. (column 6 lines 8-13). Based on this, the design templates are generated (column

6 lines 28-30), and then the blocks are implemented in a top-down method (column 6 lines 55-56). After each of the blocks has been implemented, they are compiled. Part of the compilation includes doing a schematic vs. layout check (column 7 lines 49-53). In order to do this, a layout has to be generated for each of the blocks.

c. Creating a physical schematic for said part (column 7 lines 52-57).

d. Associating said logical schematic, said layout schematic, and said physical schematic together to from a part master file (column 5 lines 41-47). The project taught by Heile contains all project files, design files, assignment files, and simulation files, among other things. *Thus, a project is functionally equivalent to the part master file claimed by the applicant.*

e. Storing said part master file on a computer network (column 8 lines 35-49)

f. Providing access to said part master file to a plurality of user locations (column 8 lines 35-49); and controlling modifications of said part master file whereby said controlling comprises allowing only one of said plurality of user locations to modify said part master file at a time (column 3 lines 19-21).

As per **claim 3**, Heile is directed to the method of claim 1, further comprising the steps of modifying said part master file and tracking a modification to said part master file (column 10 lines 20-25, 28-32, column 11 lines 1-12). The method taught by Heile allows for users to retrieve older versions of a file (column 13 lines 51-53). In order to do this, the changes that are made to a file must be tracked.

As per **claim 4**, Heile is directed to the method of claim 3, wherein said tracking comprises storing a revised part master file (column 5 lines 46-47, column 10 lines 28-32, column 13 lines 32-34). The project taught by Heile also holds a project database, which is responsible for storing intermediate data structures and version information (column 5 lines 46-47). In order to rollback to older versions of a file (column 13 lines 51-53), the original version of the file must be saved in the project, along with the new revised version.

As per **claim 5**, Heile is directed to the method of claim 3, further comprising the step of notifying an interested user location of said modifying (column 3 lines 22-26).

As per **claim 6**, Heile is directed to the method of claim 1, wherein said plurality of user locations comprises at least one remote user location (column 8 lines 42-49, 53-57).

As per **claim 8**, Heile is directed to the method of claim 1, wherein said associating is accomplished by a computer software program (column 5 lines 40-47, column 6 lines 13-15). The entire design is electronic, and all files contained within a project are associated to be part of the same design.

As per **claim 9**, Heile is directed to the method of claim 1, further comprising the steps of creating a second logical schematic for a sub-part, creating a second physical schematic for said sub-part, creating a second layout schematic for said sub-part, associating said second logical schematic, said second physical schematic and said second layout schematic together to form a

sub-part master file, and storing said sub-part master file in said part master file (column 6 lines 54-61, column 7 lines 6-13, 39-42). Heile recognizes that for complicated designs, there are multi-level block diagrams (blocks within blocks). After the top-level diagram is done, the other blocks are then implemented in an order specified by the engineer (column 7 lines 6-10). Each of the blocks is implemented using the same methodology as the top-level block (column 7 lines 11-13).

As per **claim 10**, Heile is directed to the method of claim 9, further comprising the step of controlling modification of said sub-part master file, allowing one of said plurality of user locations to modify said sub-part master file at a time (column 3 lines 19-21). The examiner interprets a sub-part master file to indicate any file that is contained within the master file. This is functionally equivalent to the global source file taught by Heile.

As per **claim 11**, Heile is directed to a system for managing electrical schematic data comprising:

a. A computer (column 25 lines 65-67, column 26 lines 1-2).
b. At least one computer aided engineering software program (column 1 lines 59-62, column 2 lines 61-66), said at least one software program being capable of creating a logical schematic (column 6 lines 54-55, column 7 lines 14-22), a layout schematic (column 7 lines 49-52), and a physical schematic (column 7 lines 52-57, 34-35) for a part based on an input into said computer from a user (column 6 lines 8-15). Heile teaches that before developing the design, a system specification for the design is

obtained. The specification includes information on the pins, system functionality, timing restraints, etc. (column 6 lines 8-13). Based on this, the design templates are generated (column 6 lines 28-30), and then the blocks are implemented in a top-down method (column 6 lines 55-56). After each of the blocks has been implemented, they are compiled. Part of the compilation includes doing a schematic vs. layout check (column 7 lines 49-53). In order to do this, a layout has to be generated for each of the blocks.

c. A computer schematic management utility, said computer schematic management utility being capable of associating said logical schematic, said layout schematic, and said physical schematic together to form a part master file (column 5 lines 40-47, column 6 lines 13-15). The project taught by Heile contains all project files, design files, assignment files, and simulation files, among other things. *Thus, a project is functionally equivalent to the part master file claimed by the applicant.* The entire design is electronic, and all files contained within a project are associated to be part of the same design.

d. A computer network, said computer network comprising said computer and a plurality of user locations, aid computer network being capable of storing said part master file and providing access to said part master file to said plurality of user locations (column 8 lines 35-49)

e. Whereby said computer schematic management utility controls modification of said part master file stored on said computer network (column 3 lines 19-26, column 10

lines 20-25, 28-35). The utility controls modifications by making sure only one user edits a global file at a time, tracking the changes, and notifying users of such changes.

As per **claim 12**, Heile is directed to the system of claim 11, wherein said computer schematic management utility controls modification of said part master file by allowing only one of said plurality of user locations to modify said part master file at a time (column 3 lines 19-21).

As per **claim 14**, Heile is directed to the system of claim 11, wherein said computer schematic management utility is further capable of tracking a modification of said part master file (column 10 lines 20-25, 28-32). The system taught by Heile allows users to retrieve older versions of a file (column 13 lines 51-53). In order to do this, the changes that are made to a file must be tracked.

As per **claim 15**, Heile is directed to the system of claim 14, wherein said tracking comprises storing a revised part master file (column 5 lines 46-47, column 10 lines 28-32, column 13 lines 32-34). The project taught by Heile also holds a project database, which is responsible for storing intermediate data structures and version information (column 5 lines 46-47). In order to rollback to older versions of a file (column 13 lines 51-53), the original version of the file must be saved in the project, along with the new revised version.

As per **claim 16**, Heile is directed to the system of claim 11, further comprising an interested user list, wherein said computer schematic management utility generates a notification to

interested user list when said part master file is modified (column 14 lines 23-34). By placing the work space in default mode, the system will automatically retrieve updated files for the user.

As per **claim 17**, Heile is directed the system of claim 16, wherein said notification comprises an electronic message (column 14 lines 23-34). By placing the work space in default mode, the system will automatically retrieve updated files for the user.

As per **claim 18**, Heile is directed to the system of claim 11, wherein said plurality of user locations comprises at least one remote user location (column 8 lines 42-49, 53-57).

As per **claim 19**, Heile is directed to a method for managing electrical schematic data comprising:

a. Creating a logical schematic for a part with a first computer aided design tool (column 6 lines 54-55, column 7 lines 14-22)
b. Creating a layout schematic for said part based on said logical schematic with a second computer aided design tool (column 7 lines 49-52). Heile teaches that before developing the design, a system specification for the design is obtained. The specification includes information on the pins, system functionality, timing restraints, etc. (column 6 lines 8-13). Based on this, the design templates are generated (column 6 lines 28-30), and then the blocks are implemented in a top-down method (column 6 lines 55-56). After each of the blocks has been implemented, they are compiled. Part

of the compilation includes doing a schematic vs. layout check (column 7 lines 49-53). In order to do this, a layout has to be generated for each of the blocks.

c. Creating a physical schematic for said part based on said logical schematic and said layout schematic with a third computer aided design tool (column 7 lines 52-57, 34-35).

d. Associating said logical schematic, said layout schematic, and said physical schematic together to form a part master file, said associating comprising storing said logical schematic, said layout schematic, and said physical schematic in a single file (column 5 lines 40-47, column 6 lines 13-15). The project taught by Heile contains all project files, design files, assignment files, and simulation files, among other things. Thus, a project is functionally equivalent to the part master file claimed by the applicant. The entire design is electronic, and all files contained within a project are associated to be part of the same design.

e. Storing said part master file on a computer network (column 8 lines 35-49)

f. Providing access to said part master file to a plurality of user locations (column 8 lines 35-49)

g. Controlling modification of said part master file, whereby said controlling comprises allowing only one of said plurality of user locations to modify said part master file at a time (column 3 lines 19-21).

As per **claim 21**, Heile is directed to the method of claim 19, further comprising the steps of modifying said part master file and tracking a modification to said part file (column 10 lines 20-

25, 28-32). The method taught by Heile allows for users to retrieve older versions of a file (column 13 lines 51-53). In order to do this, the changes that are made to a file must be tracked.

As per **claim 22**, Heile is directed to the method of claim 21, wherein said tracking comprises storing a revised part master file (column 5 lines 46-47, column 10 lines 28-32, column 13 lines 32-34). The project taught by Heile also holds a project database, which is responsible for storing intermediate data structures and version information (column 5 lines 46-47). In order to rollback to older versions of a file (column 13 lines 51-53), the original version of the file must be saved in the project, along with the new revised version..

As per **claim 23**, Heile is directed to the method of claim 21, further comprising the step of notifying an interested user location of said modifying (column 3 lines 22-26, column 14 lines 23-27).

As per **claim 24**, Heile is directed to the method of claim 19, wherein said plurality of user locations comprises at least one remote user location (column 8 lines 42-49, lines 53-57).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. **Claim** 7 **is rejected under 35 U.S.C. 103(a)** as being unpatentable over **Heile in view of Van Huben et al (US Patent No. 6,094,654)**, herein referred to as "Van Huben".

As per **claim 7**, Heile fails to teach the method of claim 1, further comprising the step of storing a pointer in said part master file, said pointer being capable of indicating a storage location of said logical schematic, said physical schematic, and said layout schematic.

Van Huben disclosed a similar method where in the case of the design data, the physical data is tracked via pointers whenever possible (Van Huben column 13 lines 20-22). The design data disclosed by Van Huben is analogous to the design files contained in the project taught by Heile.

At the time of the invention, it would have been obvious to one skilled in the art to combine the teachings of Heile and Van Huben to minimize the amount of file movement between servers

and to minimize the bottleneck caused by too many users accessing the servers (Van Huben column 13 lines 20-22).

3. **Claims 3, 13 and 20 are rejected under 35 U.S.C. 103(a)** as being unpatentable over **Heile in view of Tou et al (Knowledge-Based Approach for the Verification of CAD Database Generated by an Automatic Schematic Capture System)**, herein referred to as Tou.

As per **claims 3 and 20**, Heile teaches a method that uses a project to hold all files that are part of a design (column 5 lines 41-47). Heile fails to teach using the logical schematic, physical schematic, and layout schematic to form a schematic image file.

Tou discloses a method that uses the schematics of a design to form schematic image files (Tou page 1 section I lines 6-7, 10-12, page 2 section II lines 1-4).

At the time of the invention it would have been obvious to one skilled in the art to combine the teachings of Tou and Heile to provide a portable version of the design. The schematics produced by the engineering design aid software are not viewable across all platforms, software products, etc. By producing an image file of the schematics, users across all platforms and users who do not have the engineering design aid software can view the design. Furthermore, automating the schematic image capturing process improves the efficiency and productivity of Design Automation (Tou: section I 'Introduction' paragraph 2).

As per **claims 13**, Heile teaches a system that uses a project to hold all files that are part of a design (column 5 lines 41-47). Heile fails to teach using the logical schematic, physical schematic, and layout schematic to form a schematic image file.

Tou discloses a system that uses the schematics of a design to form schematic image files (Tou page 1 section I lines 6-7, 10-12, page 2 section II lines 1-4).

At the time of the invention it would have been obvious to one skilled in the art to combine the teachings of Tou and Heile to provide a portable version of the design. The schematics produced by the engineering design aid software are not viewable across all platforms, software products, etc. By producing an image file of the schematics, users across all platforms and users who do not have the engineering design aid software can view the design. Furthermore, automating the schematic image capturing process improves the efficiency and productivity of Design Automation (Tou: section I 'Introduction' paragraph 2).

Response to Arguments

Applicant's arguments filed 03/06/2006 have been fully considered but they are not persuasive.

Regarding the rejection of claims 1 and 11 under 35 U.S.C. 102(e) as being anticipated by Heile (US Patent No. 6,289,319):

A. The Applicants submit that forming a part master file from a logical schematic, a layout schematic, and a physical schematic is not set forth in the *Heile* reference. *However, the Examiner disagrees, because Heile discloses creating a logical schematic (column 6 lines 54-55; column 7 lines 14-22), a layout schematic (column 7 lines 49-52), and a physical schematic (column 7 lines 34-35, 52-57) and storing these in an encapsulating project (column 5 lines 41-49).* ***The 'project' in the prior art is analogous to the 'master file' in the claim language.*** *The schematics are also referred to as 'design files', 'source files', or 'programming files' in the prior art (column 7 lines 47-59). Heile discloses that the design entry and processing occurs in the context of a project. The project disclosed by Heile includes all project, source, design, simulation, and programming files.*

B. The Applicants submit that the teachings of Col. 7, lines 49-53 of the Heile reference teach away from linking all three of the logical schematic, layout schematic, and

physical schematic together. *However, the Examiner disagrees because the lines cited above are directed towards the compilation process for a traditional integrated circuit design, and does not address the association (or lack thereof) between any of the logical, layout, or physical schematics.*

Regarding the rejection of claim 7 under 35 U.S.C. 103(a) as being unpatentable over Heile in view of Van Huben (US Patent No. 6,094,654):

A. The Applicants argue that the *Van Huben* reference does not teach or suggest the further step of storing a pointer in the part master file wherein the pointer indicates a storage location of the data. *However, Van Huben discloses using pointers to track the physical data () to minimize the amount of file movement between servers (column 13 lines 20-23). A pointer, by definition, holds the address of a data object or function. Thus,* ***using pointers to track data (as claimed by the Applicants) is analogous to using pointers to indicate the storage location of the data (as taught by Van Huben).***

Regarding the rejection of claims 3, 13, and 20 under 35 U.S.C. 103(a) as being unpatentable over Heile in view of Tou ('Knowledge-Based Approach for the Verification of CAD Database Generated by an Automatic Schematic Capture System'):

A. The Applicants argue that the *Tou* reference does not teach using the design files to create a schematic image file. *However, Tou teaches an automatic schematic capture system (*section I 'Introduction' paragraph 2*). The system is designed to read and interpret electronic circuit diagrams from their images, and store the data into the computer. Thus, the system proceses the schematic images, interprets the image data, and converts the captured schematics into machine readable data files (*section III 'Errors in Captured Schematic Data' paragraph 1*).*

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is 571 272 5877. The examiner can normally be reached on 7:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shambhavi Patel
Examiner
Art Unit 2128

05/16/2006

KAMINI SHAH
SUPERVISORY PATENT EXAMINER